WHAT IS CLAIMED IS:

1. An apparatus for testing a system on a chip (SOC), the apparatus comprising:

a first SOC comprising a first hard disk controller and a first read channel;

a second SOC comprising a second hard disk controller and a second read channel;

an arbitrary waveform generator (AWG) to generate a timing signal; and

an adder in communication with the arbitrary waveform generator,

wherein the first SOC differentiates the timing signal received from the arbitrary waveform generator,

wherein the first SOC generates a write signal in synchronization with the timing signal,

wherein the adder adds the write signal from the first SOC and the timing signal to output a combined signal having a timing signal component and a write signal component; and

wherein the second SOC differentiates the timing signal component which simulates a servo signal and the write signal component simulates a signal being accessed by a read channel.

2. The apparatus of claim 1, further comprising a first host to control the first SOC and a second host to control the second SOC.

3. The apparatus of claim 1, wherein the first SOC is the same as the second SOC.

4. The apparatus of claim 1, wherein the output of the AWG is received by the first read channel.

5. The apparatus of claim 1, wherein the output of the adder is received by the second read channel.

6. An apparatus for testing a system on a chip (SOC), the apparatus comprising:

a first SOC comprising a first hard disk controller and a first read channel;

a first differentiator;

a second SOC comprising a second hard disk controller and a second read channel;

a second differentiator;

an arbitrary waveform generator (AWG) to generate a timing signal; and

an adder in communication with the arbitrary waveform generator,

wherein the first differentiator differentiates the timing signal received from the arbitrary waveform generator,

wherein the first SOC generates a write signal responsive to the first differentiator and in synchronization with the timing signal,

wherein the adder adds the write signal from the first SOC and the timing signal to output a combined signal having a timing signal component and a write signal component,

wherein the second differentiator differentiates the timing component responsive to the adder, and

wherein in the second SOC, the differentiated timing signal component from the second differentiator simulates a servo signal and the write signal component simulates a signal being accessed by a read channel.

7. The capparatus of claim 6, further comprising a first host to control the first SOC and a second host to control the second SOC.

8. The apparatus of claim 6, wherein the first SOC is the same as the second SOC.

9. The apparatus of claim 6, wherein the output of the AWG is received by the first read channel.

10. The apparatus of claim 6, wherein the output of the adder is received by the second read channel.

11. An apparatus for testing a system on a chip (SOC), the apparatus comprising:

a first SOC comprising a first means for controlling a hard disk and a first means for reading data included on a hard disk;

a second SOC comprising a second means for controlling a hard disk and a second means for reading data included on a hard disk;

a means for generating a timing signal; and

a means for adding input signals, the means for adding being in communication with the means for generating,

wherein the first SOC differentiates the timing signal received from the generating means,

wherein the first SOC generates a write signal in synchronization with the timing signal,

wherein the means for adding adds the write signal from the first SOC and the timing signal to output a combined signal having a timing signal component and a write signal component; and

wherein the second SOC differentiates the timing signal component which simulates a servo signal and the write signal component simulates a signal being accessed by a means for reading data included on a hard disk.

12. The apparatus of claim 11, further comprising a first host means for controlling the first SOC and a second host means for controlling the second SOC.

13. The apparatus of claim 11, wherein the first SOC is the same as the second SOC.

14. The apparatus of claim 11, wherein the output of the means for generating the timing signal is received by the first means for reading data.

15. The apparatus of claim 11, wherein the output of the means for adding is received by the first means for reading data.

16. An apparatus for testing a system on a chip (SOC), the apparatus comprising:

a first SOC comprising a first means for controlling a hard disk and a first means for reading data included on a hard disk;

a first means for differentiating an input signal;

a second SOC comprising a second means for controlling a hard disk and a second means for reading data included on a hard disk;

a second means for differentiating an input signal;

a means for generating a timing signal; and

a means for adding input signals, the means for adding being in communication with the means for generating,

wherein the first means for differentiating differentiates the timing signal received from the means for generating,

wherein the first SOC generates a write signal responsive to the first means for differentiating and in synchronization with the timing signal,

wherein the means for adding adds the write signal from the first SOC and the timing signal to output a combined signal having a timing signal component and a write signal component,

wherein the second means for differentiating differentiates the timing component responsive to the means for adding, and

wherein in the second SOC, the differentiated timing signal component from the second means for differentiating simulates a servo signal and the write signal component simulates a signal being accessed by a means for reading data included on a hard disk.

17. The apparatus of claim 16, further comprising a first host means for controlling the first SOC and a second host means for controlling the second SOC.

18. The apparatus of claim 16, wherein the first SOC is the same as the second SOC.

19. The apparatus of claim 16, wherein the output of the means for generating the timing signal is received by the first means for reading data.

20. The apparatus of claim 16, wherein the output of the means for adding is received by the first means for reading data.

21. A method of testing a first system on a chip (SOC), the method comprising the steps of:

generating a timing signal;

differentiating the timing signal;

generating a write signal in synchronization with the differentiated timing signal by a second SOC;

adding the write signal and the timing signal together to produce a combined signal having a write signal component and a timing signal component,

wherein the timing signal component simulates a servo signal, and the write signal component simulates a signal being accessed by a read channel; and

inputting to the first SOC the timing signal component and the write signal component.

22. The apparatus of claim 6, wherein the first SOC is the same as the second SOC.

23. The method of claim 21, wherein a first host is used for controlling the first SOC and a second host is used for controlling the second SOC.

24. A method of testing a first system on a chip (SOC), with a second SOC, the method comprising the steps of:

connecting an output of a signal generator to an input of a read channel portion of the second SOC ;

connecting an output of a write driver portion of a first SOC to a first input of a summing circuit;

connecting the output of the signal generator to a second input of a summing circuit; and

connecting the output of the adding circuit to an input of a read channel portion of the first SOC.

25 A method of Claim 24, wherein the signal generator generates a write signal in synchronization with the timing signal.

26 A method of Claim 25, wherein the summing circuit adds the write signal and the timing signal together to produce a combined signal having a write signal component and a timing signal component.

27 A method of Claim 26, wherein the second SOC differentiates the timing signal component of the combined signal, wherein the timing signal component simulates a servo signal, and wherein the write signal component simulates a signal being accessed by a read channel.

28. A method of Claim 24, wherein the first SOC is the same as the second SOC.

29. An apparatus of Claim 1, wherein the first SOC comprises a write driver to generate the write signal.

30. An apparatus of Claim 6, wherein the first SOC comprises a write driver to generate the write signal.

31. An apparatus of Claim 11, wherein the first SOC comprises a write driver means for generating the write signal.

32. An apparatus of Claim 16, wherein the first SOC comprises a write driver means for generating the write signal.